Switched Capacitor Filter

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ABSTRACT: A Switched Capacitor circuit is an electronic circuit element used for discrete time signal processing. It works by moving charges into and out of capacitors when switches are opened and closed. Usually, nonoverlapping signals are used to control the switches, so that not all switches are closed simultaneously. Filters implemented with these elements are termed switched capacitor filters. Unlike analog filters, which must be constructed with resistors, capacitors (and sometimes inductors) whose values are accurately known switched capacitor filters depend only on the ratios between capacitances. This makes them much more suitable for use with in integrated circuits, where accurately specified resistors and capacitors are not economical to construct.

Index Terms- Switched Capacitor Filter, Resistor Emulation, Switched Capacitor Integrator, Parasitic insensitive Integrator

1 Introduction

Before the advent of active elements, filters were implemented with passive elements, such as inductors, capacitors, and resistors. Practical inductors however are typically lossy, limiting the attainable selectivity. Furthermore, at low frequencies, the required size and weight of the inductors becomes large. On the other hand, very high Q can be attained with practical capacitors. Active RC filters were developed to exploit this fact and use active integrators to emulate RLC networks. Given a continuous-time transfer function, an active RC realization can be created by mapping it onto active RC integrators.

2.1 Switched Capacitor Circuits

Frequency or time precision of an analog signal processing circuits is determined by the accuracy of circuit time constants. Consider the simple first order low pass filter

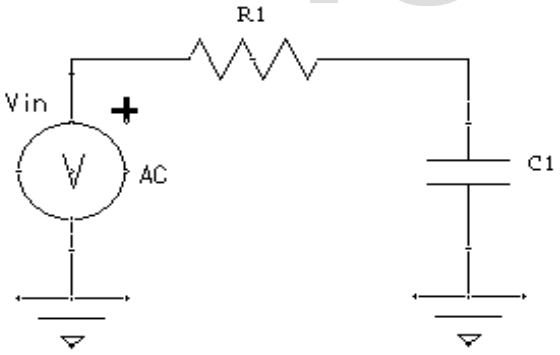


Fig 2.1 Simple 'RC' low-pass filter

Transfer function of this circuit in frequency domain:

$$H(j\omega) = \frac{V_2(j\omega)}{V_1(J\omega)} = \frac{1}{(1 + j\omega R_1 C_1)}$$

$$= \frac{1}{(1+j\omega\tau)}$$

$$\tau = R_1 C_1$$

τ = Time Constant

2.2 Resistor Emulation of Switched Capacitor

The essence of the switched-capacitor is the use of capacitors and analog switches to perform the same function as a resistor. Why one would want to replace the resistor with such an apparently complex assembly of parts as switches and capacitors. The switched-capacitor is area intensive and the use of the switched-capacitor will be seen to give frequency tunability to active filters.

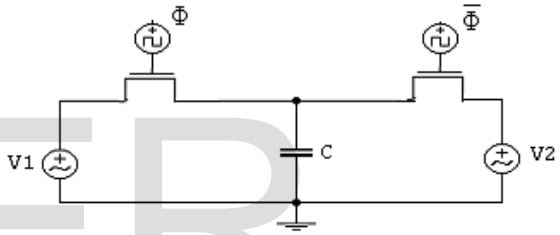


Fig 2.2 Two NMOS's, driven by alternating, non-overlapping clock

Figure 2.2 shows the basic setup for a switched-capacitor, including two N-channel Metal-Oxide Semiconductor Field-Effect Transistors (NMOS) and a capacitor. There are two clock phases, Φ and Φ', which are non-overlapping. The MOSFET's, either M1 or M2, will be turned ON when the gate voltage is high, and the equivalent resistance of the channel in that case will be low, RON → 1 KΩ → 10 KΩ. Conversely, when the gate voltage goes LOW, the channel resistance will look like ROFF ≈ 1012Ω.With such a high ratio of OFF to ON resistances, each MOSFET can be taken for a switch. Furthermore, when the two MOSFET's are driven by non-overlapping clock signals, then M1 and M2 will conduct during alternate half-cycles.

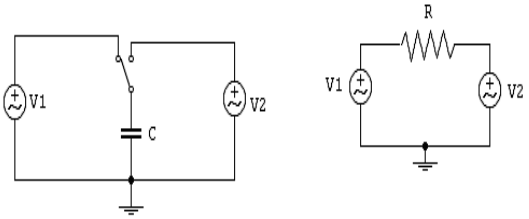


Fig. 2.3 Equivalent resistor model for switched capacitor circuit in Fig. 2.2.

The operation of this circuit is as follows. When the switch in Figure 2.3(a) is thrown to the left, the capacitor will charge up to V1. When the switch is thrown to the right, the capacitor will discharge down to/charge up to V2. As a result of these consecutive switching events, there will be a net charge transfer

$$\Delta Q = C \cdot \Delta V = C \cdot (V1 - V2)$$

Now, if one flips the switch back and forth at a rate of fclk cycles/sec, then the charge transferred in one second is

$$fCLK \cdot \Delta Q = C \cdot fCLK \cdot (V1 - V2)$$

Which has the units of current? The average current,

$$IAVG = C \cdot fCLK \cdot (V1 - V2)$$

If f clk is much higher than the frequency of the voltage waveforms, then the switching process can be taken to be essentially continuous, and the switched-capacitor can then be modelled as an equivalent resistance, as shown below in Figure 2.3(b). The value of the equivalent resistance is given by:

$$Req = \frac{V1 - V2}{I_{AVG}} = \frac{1}{C \cdot f_{CLK}} \qquad (1.1)$$

Therefore, this equivalent resistance, in conjunction with other capacitors, and Op-amp integrators, can be used to synthesize active filters. It is now clear from Equation (1.1) how the use of the switched-capacitor leads to tunability in the active filters, by varying the clock frequency.

This equivalent resistance has features which make it advantageous when realized in integrated-circuit form:

(a) High-value resistors can be implemented in very little silicon area.

(b) Very accurate time constants can be realized, because the time constant is proportional to the ratio of capacitances, and inversely proportional to the clock frequency:

$$\textit{Time constant} = Req\ C1 = \frac{C1}{C.\ f_{CLK}}$$

Capacitor ratios, especially in monolithic form, are very robust against changes in temperature, and clock frequencies can also be strictly controlled, so that accurate time constants are now available in the switched-capacitor technology.

The principal constraint in using the switched-capacitor is that inherent in all sampled-data systems: the clock frequency must be much higher than the critical frequency set by the RC products in the circuit. Furthermore, on either side of the analog switches, i.e., the MOSFET's, there must be essentially zero-impedance nodes (voltage sources).

2.3 The Switched Capacitor Integrator:

The op-amp integrator is the most frequently chosen building block for switched capacitor filters. The standard integrator is shown in figure 2.4.

The voltage transfer function of this circuit is given by

$$H(f) = \frac{Vo(f)}{Vin(f)} = -1/j(\frac{f}{f0}) \ldots\ldots\ldots\ldots\ldots (1)$$

Where

$$fo = 1/2\pi RC$$

Now, if we replace the resistor by its switched-capacitor equivalent, as shown in Figure 1.5 and use Eq. 1 as the register's value

$$fo = \frac{1\ \ C1fclk}{2\pi C2} \ldots\ldots\ldots\ldots\ldots (2)$$

This new integrator has no resistors. Which take up excessive silicon die area.Also,the -3dB frequency fo depends on a ratio of capacitances, not on an RC products. The tolerances for ratios are much easier to control than the tolerances for products. Finally, This characteristic frequency of the integrator is inherently settable with a simple change in the clock frequency.

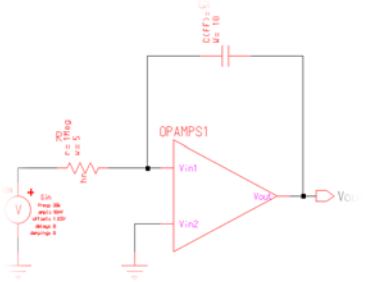


Fig. 2.4 Standard Op-amp RC integrator

Assuming an initial integrator output voltage of Vco(nT-T) implies that charge on C2 equal to C2Vco(nT-T) at time (nT-T).At time (nT-T), Φ1 is just turning off so the I/P signal Vci(t) is sampled, resulting in the charge on C1 being equal to C1 Vci(nT-T).

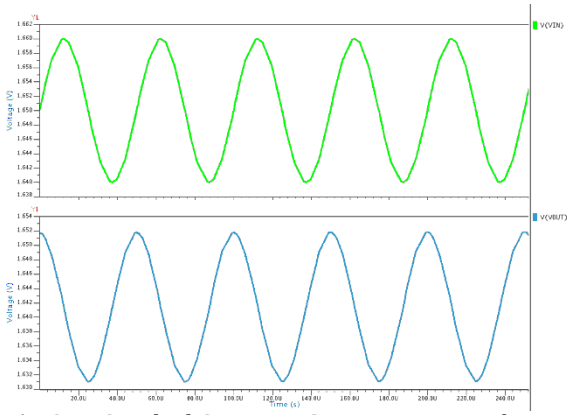


Fig. 2.4a Standard Op-amp RC integrator wave shape

When Φ2 goes high, its switch forces C1 to discharge since it places a virtual ground on the top plate of C1 in fig(b). This discharging current must pass through C2 and hence the charge on C1 is added to the charge already present on C2. A (+Ve) input voltage will result in (-Ve) voltage across C2 and therefore a (-Ve) O/P voltage, the integrator is an inverting integrator.

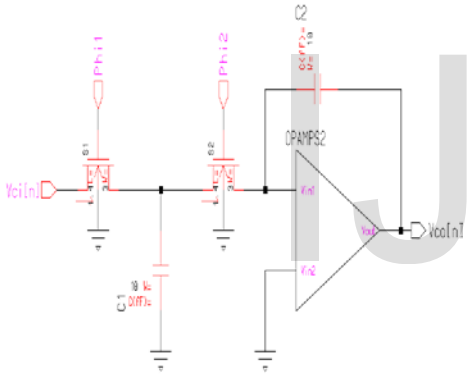


Fig. 2.5 Switched-Capacitor integrator.

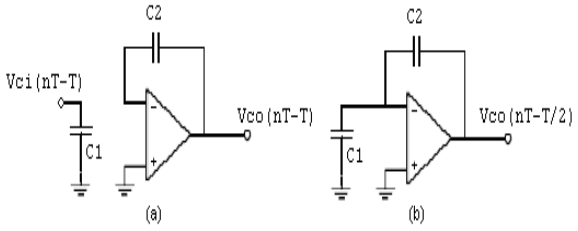


Fig. 2.6 Parasitic Sensitive Integrator for 2 clock phases (a) Φ1 (b) Φ2.

At the end of Φ2 charge equation is

C2Vco(nT-T/2)=C2Vco(nT-T)-C1Vci(nT-T) -----(3)

The (-Ve) sign reflects the fact that the integrator is an inverting integrator. Once the Φ2 turns off, the charge on C2 will remain the same during the next Φ1, until Φ2 turns ON again in its next cycle. Therefore the charge on C2 at time (nT) at the end of the next p1 is equal to that at time (nT-T/2).

C2Vco(nT)=C2Vco(nT-T/2) (4)
C2Vco(nT)=C2Vco(nT-T)-C1Vci(nT-T) (5)
Using the discrete time variable
Vi(n)=Vci(nT)andVo(n)=Vco(nT)
Vo(n)=Vo(n-1) – C1/C2 Vi(n-1)
By taking Z transform
Vo(Z)=Z-1Vo(Z) –C1/C2Z-1Vi(Z)

$$H(Z) = \frac{V0(Z)}{Vi(Z)} = -\frac{C1Z^{-1}}{C2(1-Z^{-1})}$$

This transfer function realizes its gain coefficient as the ratio of 2 capacitances and thus transfer function can be accurately defined is an integrated ckt.

2.3.1 Effect of Parasitic Capacitor

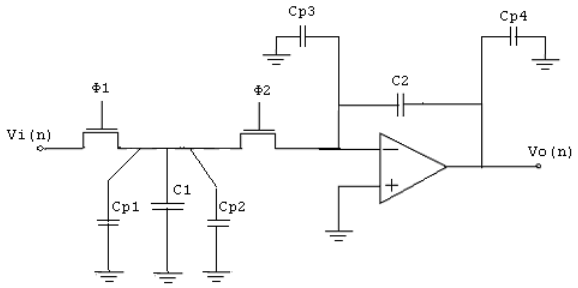


Fig 2.7 A discrete time integrator with parasitic capacitances

The additions of parasitic capacitances result in ckt. shown in fig.2.7 Cp1 represents the parasitic capacitance of the top plate of C1 as well as the nonlinear capacitance associated with 2 switches, Cp2 represents the parasitic capacitance of the bottom plate of C1, while Cp3 represents the parasitic capacitances associated with the top plate of C2, the I/P of the Op-Amp and that of the 2 switch. Finally Cp4 accounts for the bottom plate parasitic capacitance of C2 as well as any extra capacitance that the Op-Amp o/p must drive.

We can discard the effect of Cp2 since it always remains connected to ground. The effect of Cp3 on the transfer function is small since it is always connected to the virtual ground of the Op-Amp. Cp4 is connected to the Op-amp output, although it may affect the speed of Op-amp, it would not affect the final settling point of Op-amp o/p. Finally we note that Cp1 is in parallel with C1 and therefore the transfer function of this discrete time integrator including the effects of parasitic capacitances is given by

$$H(Z) = \frac{V0(Z)}{Vi(Z)} = -\frac{(C1 + Cp1)Z}{C2(Z-1)}$$

The gain coefficient is related to the parasitic coefficient Cp1, which is not well controlled and would be partially nonlinear due to the I/P capacitances of switches and top plate parasitic capacitances. The overcome this deficiency circuit known as parasitic insensitive structures were developed.

2.3.2. Parasitic Insensitive Integrator

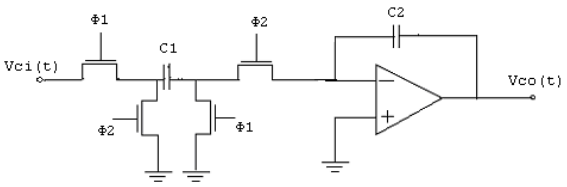


Fig. 2.8 A noninverting delaying discrete time integrator

To realizes a parasitics insensitive discrete time integrator, two extra switches are used. When Φ1 is ON, C1 is charged to C1 Vci(nT-T) as shown in fig. 1.6(a).

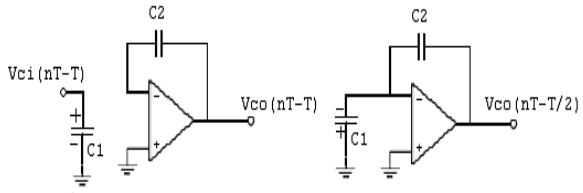


Fig.2.9 The noninverting delaying discrete time integrator on the two clock phases (a) Φ1, (b) Φ2

When Φ2 turns ON, C1 is effectively hooked up backwards and discharge now occurs through what was the ground node rather than the I/P signal side as shown in fig.1.9(b). Such a reverse connection result in Vco(t) rising for a (+Ve) Vci(nT-T) and therefore the integrator is noninverting.

The transfer function H(z) for this discrete time integrator is

$$H(Z) = \frac{V0(Z)}{Vi(Z)} = -\frac{C1Z^{-1}}{C2(1-Z^{-1})}$$

This equations represent the (+Ve) discrete time integrator with a fully delay from I/P to o/p.

$$H(Z) = \frac{V0(Z)}{Vi(Z)} = -\frac{C1\,Z}{C2(Z-1)}$$

2.3.3 Inverting Parasitic Insensitive Integrator

To obtain an inverting discrete time integrator that is also parasitic insensitive the same ckt. as parasitic insensitive noninverting integrator can be used with the 2 switch phases on the switches near the I/P side of C1 interchanged . The charge on C2 does not change when Φ2 turns ON.

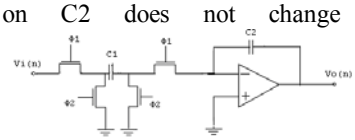


Fig. 2.10 Circuit of Inverting Parasitic Insensitive Integrator

C2Vco(nT-T/2)=C2Vco(nT-T) (6)

At the end of Φ2 ON C1 is fully discharge .When phi1is turned ON c1 is charged up to Vci(t). The current needed to charge C1 passes through C2, in effect changing the charge on C2 by that amount. At the end of Φ1 ON, the charge left on C2 is equal to its old charge subtracted from the charge needed to charge up c1 to Vci(nT).

C2Vco(nT)=C2Vco(nT-T/2)-C1Vci(nT) (7)

Substitute The eq(2) in eq(1) , divide by C2 and switching to discrete time variables

Vo(n)=Vo(n-1)–C1/C2 Vi(n)

By taking Z transform, the transfer function of this delay free integrator

$$H(Z) = \frac{V0(Z)}{Vi(Z)} = -\frac{C1}{C2(1-Z^{-1})}$$

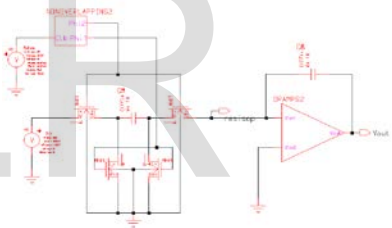
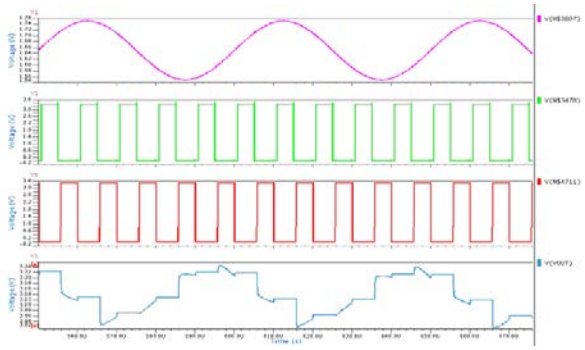


Fig. 2.11 Schematic of Inverting Parasitic Insensitive Integrator



Transient Result:

Fig. 2.12 Result of Inverting Parasitic Insensitive Integrator

3 References:

[1] P. E. Allen and D. R. Hollberg, CMOS Analog Circuit Design. Oxford University Press, second ed., 2002.
[2] B. Razavi, Design of Analog CMOS Integrated Circuits. McGraw-Hill, first ed., 1999.

[3] R. J. Baker, H. W. Li, and D. E. Boyce, CMOS Circuit Design, Layout, and Simulation. Institute of Electrical and Electronics Engineer, Inc., 1998.
[4] R. Van de Plassche, CMOS Integrated Analog-to-Digital and Digital-to- Analog Converters. Kluwer Academic Publishers, second ed., 2003.
[5] A. L. Coban and P. E. Allen, "A 1.5v, 1mW audio ΔΣ modulator with 98 dB dynamic range," Proceedings of the International Solid-State Conference, pp. 50–51, 1999.
[6] D. Johns and K. Martin, Analog Integrated Circuit Design. John Wiley & Sons, Inc., 1997.
[7] Texas Instruments, Data Converter Selection Guide, 2004.
ZZZ[8] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits. John Wiley & Sons, Inc., third edition ed., 1993.
[9] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," IEEE Journal of Solid-State Circuits, vol. 27, no. 12, pp. 1916–1926, 1992.
[10] J. Park, J.-W. Kim, S. Seo, and P. Chung, "A 1 mW 10-bit 500 KSPS SAR A/D converter," IEEE International Symposium on Circuits and Systems, pp. 581–584, 2000.
[11] H. Neubauer, T. Desel, and H. Hauer, "A successive approximation A/D converter with 16bit 200kS/s in 0.6um CMOS using self calibration and low power techniques,"

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